Notic of Allowability	Application N .	Applicant(s)	
	10/840,154	FAHS ET AL.	
	Examin r	Art Unit	
	Than Nguyen	2187	

-- The MAILING DATE of this communication appears on th cover sheet with the c rrespondenc address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *5/5/04*.

2. ☒ The allowed claim(s) is/are *1-10*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. Claims 1-10 are pending.

Examiner's Amendment

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee. Authorization for this examiner's amendment was given in a telephone interview with Philip McKay on 6/7/06.

The application has been amended as follows:

In the claims

2. Claim 7, line 2. Replace "1" with --6--.

Allowable Subject Matter

3. Claims 1-10 are allowed.

4. The following is an examiner's statement of reasons for allowance (emphasis in bold):

5. As to claim 1, the prior art does not suggest a method for monitoring prefetches due to speculative accesses in a computer system comprising: providing a processor for processing data; providing a cache memory, said cache memory capable of being accessed by said processor; providing an off-chip memory system, said off-chip memory system capable of being accessed by said processor; providing for speculative accesses by said processor to transfer data from said off-chip memory system to said cache memory system; **modifying said processor such that**

said processor is capable of determining and labeling accesses as speculative and said processor is capable of indicating to said cache memory whether an access is speculative or non-speculative; providing said processor with a programmable prefetch counter that can be set, said prefetch counter for counting the number of prefetches, said prefetch counter providing said processor with the ability to trap on the occurrence of a predetermined state of said prefetch counter; providing a bit per tag called an S-bit, said S-bit indicating whether a cache line was accessed speculatively, wherein; a speculative insert of a cache line causes the S-bit of the cache line to be set, thereby changing the state of the cache line to the speculative state, further wherein; a speculative update of a cache line results in the setting of the S-bit of the updated cache line, thereby changing the state of the cache line to the speculative state, further wherein; a speculative miss of a cache line results in no change, further wherein; a non-speculative insert of a cache line results in the S-bit of the inserted cache line being cleared and the state of the cache line to be changed to the non-speculative state, further wherein; a non-speculative update of a cache line results in incrementing the prefetch count of said programmable prefetch counter if the updated cache line S-bit is set and the clearing of the S-bit of the cache line to the non-speculative state, further wherein; a non-speculative miss of a cache line results in no change.

6. As to claim 4, the prior art does not suggest a method for monitoring prefetches due to speculative accesses in a computer system comprising: providing a processor for processing data; providing a cache memory, said cache memory capable of being accessed by said processor; providing an off-chip memory system, said off-chip memory system capable of being accessed by said processor; providing for speculative accesses by said processor to transfer data from said

off-chip memory system to said cache memory system; **modifying said processor such that said processor is capable of determining and labeling accesses as speculative and said processor is capable of indicating to said cache memory whether an access is speculative or non-speculative; providing said processor with a programmable prefetch counter that can be set, said programmable prefetch counter for counting the number of prefetches, said programmable prefetch counter providing said processor with a table to hold instruction addresses called an instruction address table (IAT), wherein, the instruction address of a prefetched instruction is stored in the IAT; providing said processor with the ability to trap according to a predetermined condition of said programmable prefetch counter, wherein, when a trap occurs a sample is taken from said prefetch occurrence that caused the trap; providing a bit per tag called an S-bit, said S-bit indicating whether a cache line was accessed speculatively, wherein; a speculative insert of a cache line causes the S-bit of the cache line to be set, thereby changing the state of the cache line to the speculative state, and the address to be stored, further wherein; a speculative update of a cache line results in the setting of the S-bit of the updated cache line, thereby changing the state of the cache line to the speculative state, further wherein; a speculative miss results in no change, further wherein; a non-speculative insert of a cache line results in the S-bit of the inserted cache line being cleared, thereby changing the state of the cache line to the non-speculative state, further wherein; a non-speculative update of a cache line results in incrementing the prefetch count of said programmable prefetch counter, the clearing of the S-bit if the updated cache line S-bit is set and, if said prefetch counter reaches said predetermined state and the present instruction caused the predetermined state, a trap is initiated, the**

address of the instruction that caused the trap is supplied from the IAT, and the data address of the prefetched cache line is supplied, further wherein; a non-speculative miss results in no change.

7. As to claim 6, the prior art does not suggest a method for monitoring pollutions due to speculative accesses in a computer system comprising: providing a processor for processing data; providing a cache memory, said cache memory capable of being accessed by said processor; providing an off-chip memory system, said off-chip memory system capable of being accessed by said processor; providing for speculative accesses by said processor to transfer data from said off-chip memory system to said cache memory system; **modifying said processor such that said processor is capable of determining and labeling accesses as speculative and said processor is capable of indicating to said cache memory whether an access is speculative or non-speculative; providing said processor with a programmable prefetch counter that can be set, said programmable prefetch counter for counting the number of prefetches, said programmable prefetch counter providing said processor with the ability to trap on the occurrence of a predetermined state of said prefetch counter; providing a bit per tag called an S-bit, said S-bit indicating whether a cache line was accessed speculatively; providing a bit per tag called an A-bit, said A-bit indicating whether a cache line was affected by a speculative access; providing a table called an evicted tag table (ETT), said ETT containing one tag entry per cache set, entries in said ETT being used to store the most recently evicted cache line in the case that it was evicted because a speculative access occurred; providing a pollution counter to count the number of pollutions; providing instructions to read and clear said pollution counter; modifying said processor such that said processor**

traps upon a predetermined state of said pollution counter, wherein; a speculative insert of a cache line causes the S-bit of the cache line to be set, thereby changing the state of the cache line to the speculative state, the A-bit to be set of all other cache lines that do not have their S-bits set, thereby changing the state of all other cache lines that do not have their S-bits set to A-state, and the tag of the evicted cache line is moved to the ETT entry for this set, further wherein; a speculative update of a cache line results in the setting of the S-bit of the updated cache line, thereby changing the state of the cache line from the non-speculative state to the speculative state and, if this access modifies the replacement ordering of the cache set, then the A-bits of all cache lines that had their replacement ordering modified are set and their S-bits are set to zero, further wherein; a speculative miss of a cache line results in no change, further wherein; a non-speculative insert of a cache line results in the S-bit of the inserted cache line being cleared and the state of the cache line being set to the non-speculative state and, if the evicted entry has the A-bit set, then the tag of the evicted cache line is moved to the ETT entry for the cache set, further wherein; a non-speculative update of a cache line results in incrementing the prefetch count of said programmable prefetch counter if the updated cache line S-bit is set, the clearing of the S-bit, thereby changing the state of the cache line to the non-speculative state, clearing of the A-bit of all other cache lines, thereby changing the state of all other cache lines to the non-speculative state, and invalidating the ETT entry for this cache set, further wherein; a non-speculative update of a cache line results in a change of state from the A-state to the non-speculative state, further wherein; in the event of a non-speculative miss of a cache line, if the ETT entry for the set is valid and equals the tag of the accessed

cache line, then the pollution count of said pollution counter is incremented and the ETT entry for this cache set is cleared.

8. As to claim 9, the prior art does not suggest a method for monitoring pollutions due to speculative accesses in a computer system comprising: providing a processor for processing data; providing a cache memory, said cache memory capable of being accessed by said processor; providing an off-chip memory system, said off-chip memory system capable of being accessed by said processor; providing for speculative accesses by said processor to transfer data form said off-chip memory system to said cache memory system; **modifying said processor such that said processor is capable of determining and labeling accesses as speculative and said processor is capable of indicating to said cache memory whether an access is speculative or non-speculative; providing said processor with a programmable prefetch counter that can be set, said programmable prefetch counter for counting the number of prefetches, said programmable prefetch counter providing said processor with a table to hold instruction addresses called an instruction address table (IAT), wherein, the instruction address of a prefetched instruction is stored in the IAT; providing said processor with the ability to trap on the occurrence of a predetermined state of said prefetch counter, wherein, when said prefetch counter reaches said predetermined state, a trap occurs and a sample is taken from said prefetch that caused said trap; providing a bit per tag called an S-bit, said S-bit indicating whether a cache line was accessed speculatively; providing a bit per tag called an A-bit, said A-bit indicating whether or not a cache line was affected by a speculative access; providing a table called an evicted tag table (ETT), said ETT containing one tag entry per cache set, entries in said ETT being used to store the most recently evicted cache line in the**

case that it was evicted because a speculative access occurred; providing a pollution counter to count the number of pollutions; providing instructions to read and clear said pollution counter; modifying said processor such that said processor traps upon said predetermined state of said pollution counter, wherein; a speculative insert of a cache line causes the S-bit of the cache line to be set, thereby changing the state of the cache line to the speculative state, the A-bit to be set of all other cache lines that do not have their S-bits set, thereby changing the state of all other cache lines that do not have their S-bits set to A-state, the tag of the evicted cache line is moved to the ETT entry for the set and, the instruction address to be stored, further wherein; a speculative update of a cache line results in the change of state from the A-state to the speculative state, further wherein; a speculative update of a cache line results in the setting of the S-bit of the updated cache line, thereby changing the state of the cache line from the non-speculative state to the speculative state and, if the access modifies the replacement ordering of the cache set, then the A-bits of all cache lines that had their replacement ordering modified are set and their S-bits are set to zero, further wherein; a speculative miss results in no change, further wherein; a non-speculative insert of a cache line results in the S-bit of the inserted cache line being cleared, thereby changing the state of the cache line to the non-speculative state, and if the evicted entry has the A-bit set, then the tag of the evicted cache line is moved to the ETT entry for this cache set, further wherein; a non-speculative update of a cache line results in incrementing the prefetch count of said programmable prefetch counter if the updated cache line S-bit is set, clearing the S-bit, thereby changing the state of the cache line to the non-speculative state, clearing the A-bit of all other cache lines, thereby

changing the state of all other cache lines to the non-speculative state, invalidating the ETT entry for this cache set, supplying the instruction address, and supplying the data address, further wherein; a non-speculative update of a cache line results in a change of state from the A-state to the non-speculative state; and a non-speculative miss of a cache line results in the pollution count of said pollution table being incremented, the ETT entry for the cache set being cleared, the instruction address being supplied, and the data address being supplied.

9. Claims 2,3,5,7,8,10 are also allowable for incorporating the limitations of the parent claim, and further limitations.

10. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Than Nguyen whose telephone number is 571-272-4198. The examiner can normally be reached on 8am-3pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Than Nguyen
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